

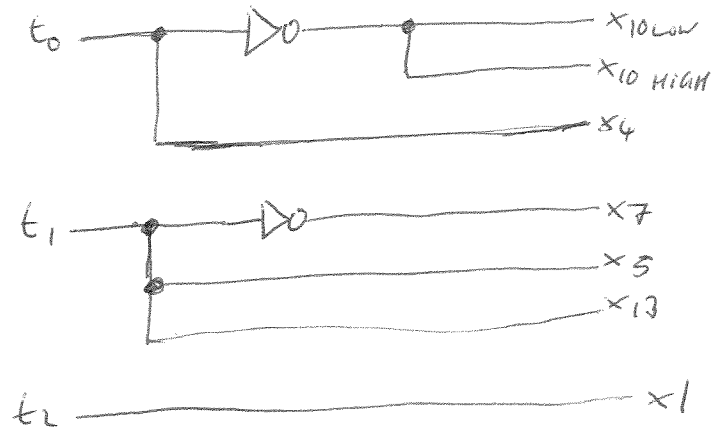
Instructions

- are in memory now
- need to encode them as bit patterns

	8 bit	
	opcode 4 bit	address 4 bit
LDA	0001	x
LDS	0010	x
STA	0011	x
SPI	0100	x
ADD	0101	x
SUB	0110	x
JMP	0111	x
JMB	1000	x

Fetch cycle identical for all instructions

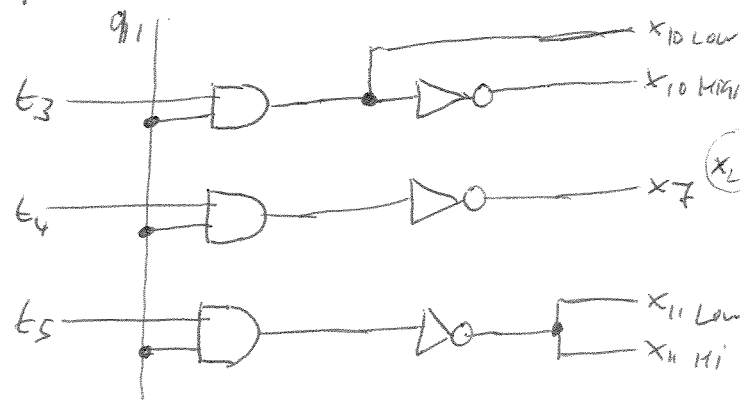
- $t_0$  MAR  $\leftarrow$  PC
- $t_1$  MBR  $\leftarrow$  MEM, PC  $\leftarrow$  PC+1
- $t_2$  IR  $\leftarrow$  MBR



Execute cycle depends on instruction, so q is relevant

LDA 0001 q1

- $q_1 t_3$  MAR  $\leftarrow$  IR(a)
- $q_1 t_4$  MBR  $\leftarrow$  MEM
- $q_1 t_5$  AC  $\leftarrow$  MBR



LDI 0010 q2

- $q_2 t_3$  MAR  $\leftarrow$  IR(a)
- $q_2 t_4$  MBR  $\leftarrow$  MEM
- $q_2 t_5$  MAR  $\leftarrow$  MBR
- $q_2 t_6$  MBR  $\leftarrow$  MEM
- $q_2 t_7$  AC  $\leftarrow$  MBR

ADD 0101 q5

- $q_5 t_3$  MAR  $\leftarrow$  IR(a)
- $q_5 t_4$  MBR  $\leftarrow$  MEM
- $q_5 t_5$  AD  $\leftarrow$  MBR
- $q_5 t_6$  AD  $\leftarrow$  AD+AC
- $q_5 t_7$  AC  $\leftarrow$  AD

JMP 0111 q7

- $q_7 t_3$  AC  $\leftarrow$  PC
- $q_7 t_4$  AD  $\leftarrow$  AC
- $q_7 t_5$  AC  $\leftarrow$  IR(a)
- $q_7 t_6$  AD  $\leftarrow$  AD+AC
- $q_7 t_7$  AC  $\leftarrow$  AD
- $q_7 t_8$  PC  $\leftarrow$  AC

(2)

